

Clock Buffer/Clock Multiplier With Optional SSC

Check for Samples: [CDCS503-Q1](#)

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 2
 - -40°C to +105°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H2
 - Device CDM ESD Classification Level C3B
- Part of a Family of Easy to use Clock Generator Devices With Optional SSC
- Clock Multiplier With Selectable Output Frequency and Selectable SSC
- SSC Controllable via 2 External Pins
 - ±0%, ±0.5%, ±1%, ±2% Center Spread
- Frequency Multiplication Selectable Between x1 or x4 With One External Control Pin
- Output Disable via Control Pin

- Single 3.3V Device Power Supply
- Wide Temperature Range –40°C to 105°C
- Low Space Consumption 8-Pin TSSOP Package

APPLICATIONS

- Automotive Applications requiring EMI reduction through Spread Spectrum Clocking and/ or Clock Multiplication

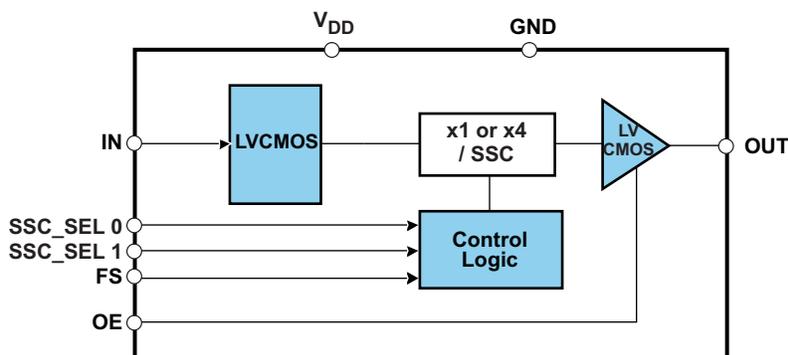


Figure 1. BLOCK DIAGRAM

PRODUCT PREVIEW


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DESCRIPTION

The CDCS503-Q1 is a spread spectrum capable, LVCMOS Input Clock Buffer with selectable frequency multiplication.

It shares major functionality with the CDCS502 but utilizes a LVCMOS input stage instead of the crystal input stage of the CDCS502. Also an Output Enable pin has been added to the CDCS503-Q1.

The device accepts a 3.3V LVCMOS signal at the input.

The input signal is processed by a PLL, whose output frequency is either equal to the input frequency or multiplied by the factor of 4.

The PLL is also able to spread the clock signal by $\pm 0\%$, $\pm 0.5\%$, $\pm 1\%$ or $\pm 2\%$ centered around the output clock frequency with a triangular modulation.

By this, the device can generate output frequencies between 8MHz and 108MHz with or without SSC.

A separate control pin can be used to enable or disable the output. The CDCS503-Q1 operates in 3.3V environment.

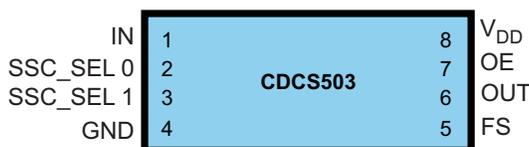
It is characterized for operation from -40°C to 105°C , and available in an 8-pin TSSOP package.

Table 1. FUNCTION TABLE

OE	FS	SSC_SEL 0	SSC_SEL 1	SSC AMOUNT	f_{OUT}/f_{IN}	f_{OUT} at $f_{in} = 27 \text{ MHz}$
0	x	x	x	x	x	3-state
1	0	0	0	$\pm 0.00\%$	1	27 MHz
1	0	0	1	$\pm 0.50\%$	1	27 MHz
1	0	1	0	$\pm 1.00\%$	1	27 MHz
1	0	1	1	$\pm 2.00\%$	1	27 MHz
1	1	0	0	$\pm 0.00\%$	4	108 MHz
1	1	0	1	$\pm 0.50\%$	4	108 MHz
1	1	1	0	$\pm 1.00\%$	4	108 MHz
1	1	1	1	$\pm 2.00\%$	4	108 MHz

DEVICE INFORMATION

PACKAGE



PIN FUNCTIONS

SIGNAL	PIN	TYPE	DESCRIPTION
IN	1	I	LVCMOS Clock input
OUT	6	O	LVCMOS Clock Output
SSC_SEL 0, 1	2, 3	I	Spread Selection Pins, internal pull-up
OE	7	I	Output Enable, internal pull-up
FS	5	I	Frequency Multiplication Selection, internal pull-up
V_{DD}	8	Power	3.3V Power Supply
GND	4	Ground	Ground

PRODUCT PREVIEW

PACKAGE THERMAL RESISTANCE FOR TSSOP (PW) PACKAGE

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PW 8-PIN TSSOP			THERMAL AIRFLOW (CFM)				UNIT
			0	150	250	500	
R _{θJA}	High K		149	142	138	132	°C/W
	Low K		230	185	170	150	
R _{θJC}	High K	65					°C/W
	Low K	69					

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V _{DD}	Supply voltage range	-0.5 to 4.6	V
V _{IN}	Input voltage range ⁽¹⁾	-0.5 to 4.6	V
V _{out}	Output voltage range ⁽¹⁾	-0.5 to 4.6	V
I _{IN}	Input current (V _I < 0, V _I > V _{DD})	20	mA
I _{out}	Continuous output current	50	mA
T _{ST}	Storage temperature range	-65 to 150	°C
T _J	Maximum junction temperature	125	°C
ESD Rating	Human-body model (HBM) AEC-Q100 Classification Level H2	1.5	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C3B	750	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage	3.0		3.6	V
f _{IN}	Input frequency	FS = 0	8	32	MHz
		FS = 1	8	27	
V _{IL}	Low level input voltage LVCMOS			0.3 V _{DD}	V
V _{IH}	High level input voltage LVCMOS	0.7 V _{DD}			V
V _I	Input voltage threshold LVCMOS		0.5 V _{DD}		V
C _L	Output load test LVCMOS			15	pF
I _{OH} /I _{OL}	Output current			±12	mA
T _A	Operating free-air temperature	-40		105	°C

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
IDD	Device supply current	f _{out} = 20 MHz; FS = 0, no SSC		19		mA	
		f _{out} = 70 MHz; FS = 1, SSC = 2%		22			
f _{OUT}	Output frequency	FS = 0		8	32	MHz	
		FS = 1		32	108		
I _{IH}	LVCMOS input current	V _I = V _{DD} ; V _{DD} = 3.6 V		10		μA	
I _{IL}	LVCMOS input current	V _I = 0 V; V _{DD} = 3.6 V		-10		μA	
V _{OH}	LVCMOS high-level output voltage	I _{OH} = -0.1mA		2.9		V	
		I _{OH} = -8mA		2.4			
		I _{OH} = -12mA		2.2			

DEVICE CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OL} LVC MOS low-level output voltage	I _{OL} = 0.1mA			0.1	V
	I _{OL} = 8mA			0.5	
	I _{OL} = 12mA			0.8	
I _{OZ} High- impedance-state output current	OE = Low	-2		2	μA
t _{JIT(C-C)} Cycle to cycle jitter ⁽¹⁾	f _{out} = 108 MHz; FS = 1, SSC = 1%, 10000 Cycles		110		ps
t _r /t _f Rise and fall time ⁽¹⁾	20%–80%		0.75		ns
O _{dc} Output duty cycle		45%		55%	
f _{MOD} Modulation frequency			30		kHz

(1) Measured with Test Load, see Figure 3.

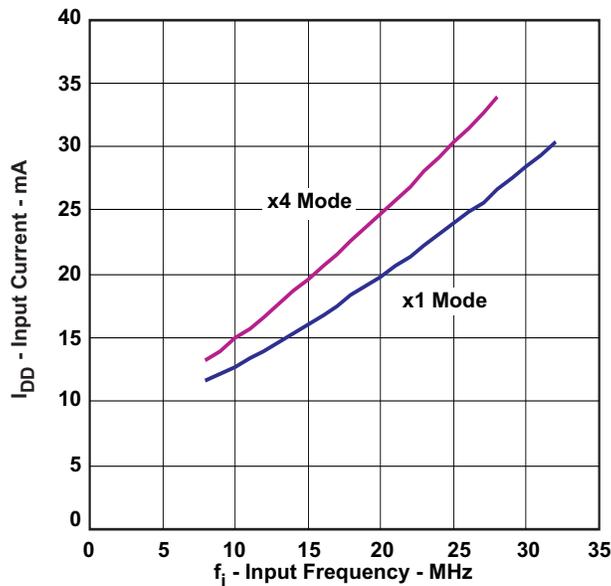


Figure 2. IDD vs Input Frequency, VCC = 3.3V, SSC = 2%, Output Loaded With Test Load

PRODUCT PREVIEW

APPLICATION INFORMATION

SSC MODULATION

The exact implementation of the SSC modulation plays a vital role for the EMI reduction. The CDCS503-Q1 uses a triangular modulation scheme implemented in a way that the modulation frequency depends on the VCO frequency of the internal PLL and the spread amount is independent from the VCO frequency.

The modulation frequency can be calculated by using one of the below formulas chosen by frequency multiplication mode.

$$FS = 0: f_{\text{mod}} = f_{\text{IN}} / 708$$

$$FS = 1: f_{\text{mod}} = f_{\text{IN}} / 620$$

PARAMETER MEASUREMENT INFORMATION

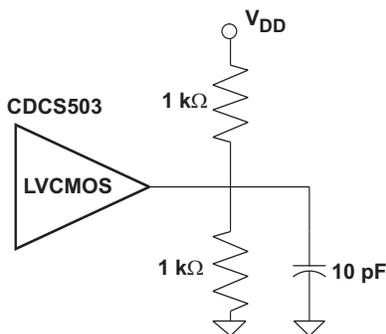


Figure 3. Test Load

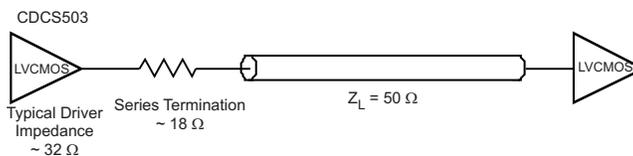


Figure 4. Load for 50-Ω Board Environment

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CDCS503IPWRQ1	PREVIEW	TSSOP	PW	8	2000	TBD	Call TI	Call TI	
CDCS503TPWRQ1	PREVIEW	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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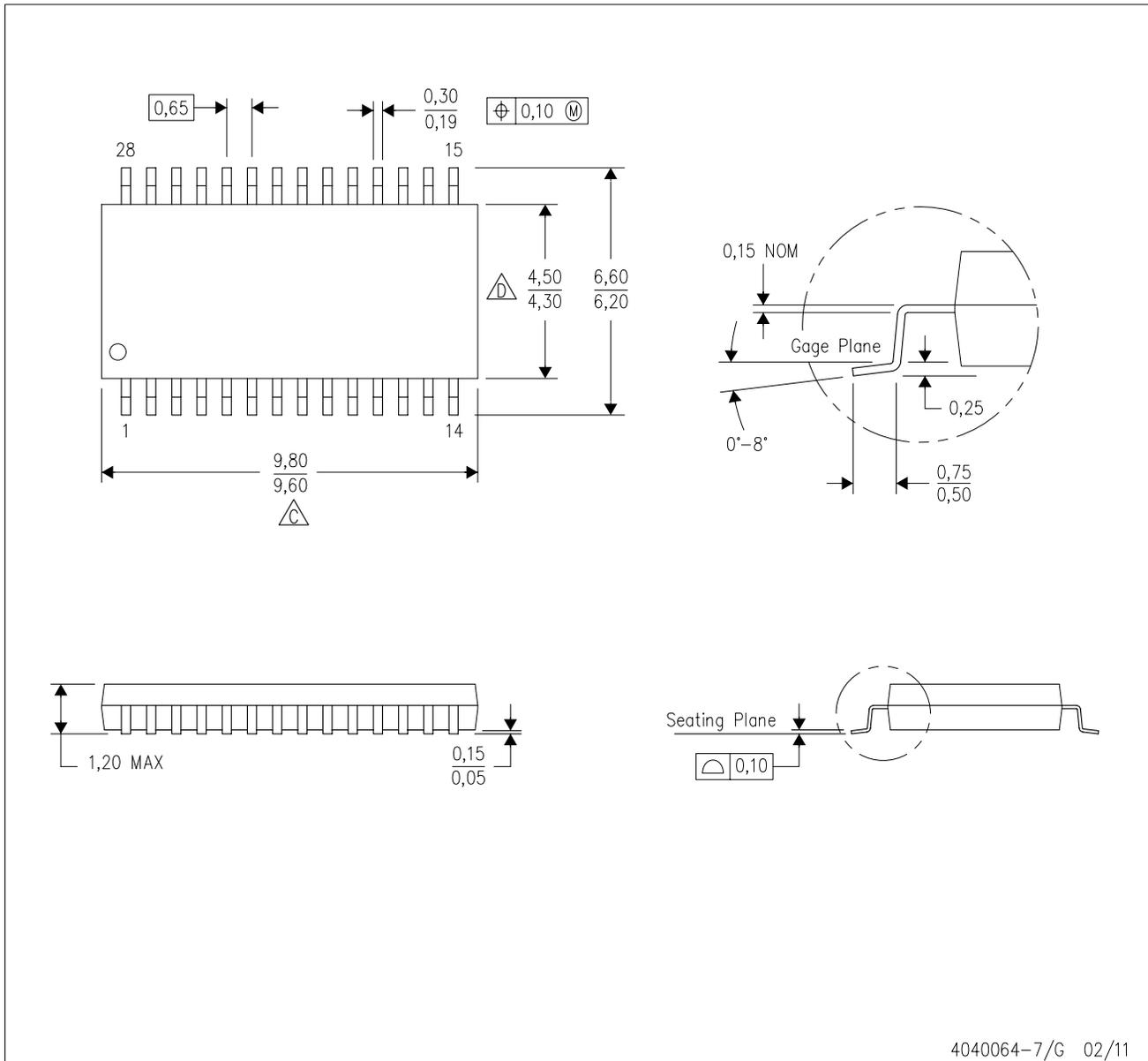
- Catalog: [CDCS503](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

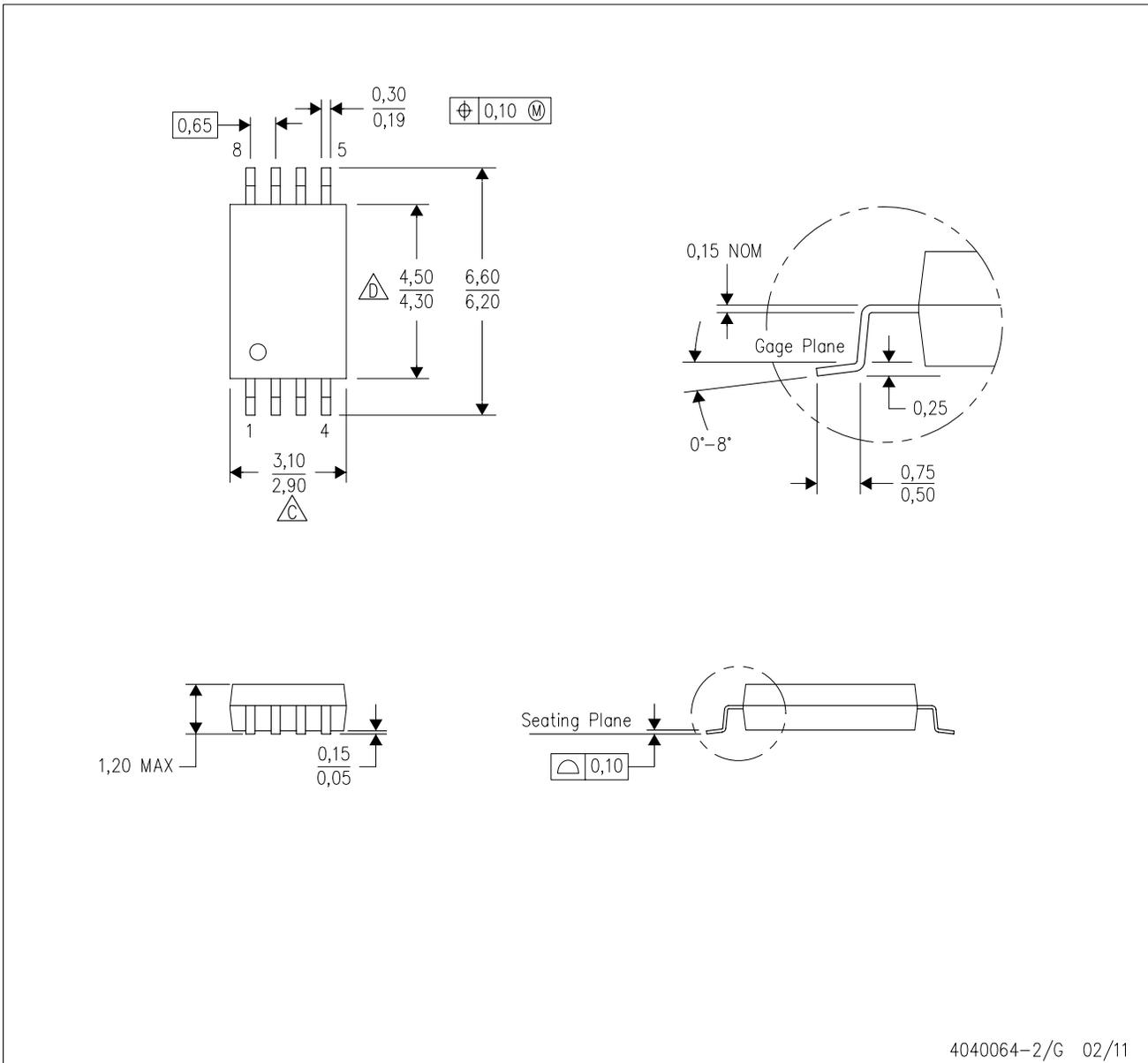


4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
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 - B. This drawing is subject to change without notice.
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 - E. Falls within JEDEC MO-153

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